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Simple Bus Architecture

- A simplified motherboard of a personal computer (top view):
Simplified Illustration of a Bus

- CPU
- Memory
- Disk

- Control ($C_0 - C_9$)
- Address ($A_0 - A_{31}$)
- Data ($D_0 - D_{31}$)
- Power (GND, +5V, −15V)
100 MHz Bus Clock
The Synchronous Bus

- Timing diagram for a synchronous memory read (adapted from [Tanenbaum, 1999]).
The Asynchronous Bus

- Timing diagram for asynchronous memory read (adapted from [Tanenbaum, 1999]).

Address

MREQ

RD

MSYN

Data

SSYN

Memory address to be read

Data valid

Time
Bus Arbitration

- (a) Simple centralized bus arbitration; (b) centralized arbitration with priority levels; (c) decentralized bus arbitration.  
  (Adapted from [Tanenbaum, 1999]).
Bridge Based Bus Architecture

- Bridging with dual Pentium II Xeon processors on Slot 2.

(Source: http://www.intel.com.)
Programmed I/O
Flowchart for a Disk Transfer

Enter

Check status of disk

No

Disk ready?

Yes

Send data from memory to disk (when writing) or from disk to memory (when reading).

No

Done?

Yes

Continue
Interrupt Driven I/O Flowchart for a Disk Transfer

1. Enter
2. Issue read or write request to disk.
3. Do other processing, until disk issues an interrupt.
   - Interrupt causes current processing to stop.
4. Transfer data between disk and memory.
   - Return from interrupt. Normal processing resumes.
5. Done?
   - Yes: Continue
   - No: Go back to step 2.
DMA Transfer from Disk to Memory
Bypasses the CPU

Without DMA

With DMA

Bus
DMA Flowchart for a Disk Transfer

1. Enter
2. CPU sets up disk for DMA transfer
3. DMA device begins transfer independent of CPU
4. DMA device interrupts CPU when finished
5. CPU executes another process
6. Continue
Intel Memory and I/O Address Spaces

Memory Space

Address

FFFFFFFFF

00000000

I/O Space

Address

FFFF

0000
Standard Intel Pentium Read and Write Bus Cycles

- **CLK**
- **ADDR**
  - Valid
  - Invalid
  - Valid
  - Invalid
- **ADS#**
- **CACHE#**
- **W/R#**
  - Read
  - Write
- **BRDY#**
- **DATA**
  - TO CPU
  - FROM CPU

**TIMING CYCLES**
- **T1**
- **T2**
- **Ti**

**STAGES**
- **READ CYCLE**
- **IDLE**
- **WRITE CYCLE**
- **IDLE**
Intel Pentium Burst Read Bus Cycle

CLK: T1, T2, T2, T2, T2, T2, Ti

ADDR: Valid, Invalid

ADS#: 

CACHE#: 

W/R#: Read

BRDY#: 

DATA: TO CPU, TO CPU, TO CPU, TO CPU

READ, READ, READ, READ
Intel Pentium Hold-Hold Acknowledge Bus Cycle
A Magnetic Disk with Three Platters

- Top surface not used
- Surface 3
- Surface 2
- Surface 1
- Surface 0
- Bottom surface not used
- Spindle
- Comb
- Head
- Air cushion
- Surface
- Read/write head (1 per surface)
- Direction of arm (comb) motion
- 5 µm
Manchester Encoding

- (a) Straight amplitude (NRZ) encoding of ASCII ‘F’; (b) Manchester encoding of ASCII ‘F’.

(a) Time

<table>
<thead>
<tr>
<th>Voltage</th>
<th>1 0 0 0 1 1 1 0</th>
<th>= ‘F’</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(b) Voltage

<table>
<thead>
<tr>
<th>1 0 0 0 1 1 1 0</th>
<th>= ‘F’</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td></td>
</tr>
</tbody>
</table>
Organization of a Disk Platter with a 1:2 Interleave Factor

Inter-sector gap

Inter-track gap

Interleave factor 1:2

Sector

Track
Master Control Block

No. surfaces on disk = 4
No. tracks/surface = 814
No. sectors/track = 32
No. bytes/sector = 512
Interleave factor = 1:3

Starting sector, or sector list

<table>
<thead>
<tr>
<th>Filename</th>
<th>Surface</th>
<th>Track</th>
<th>Sector</th>
<th>Creation Date</th>
<th>Last Modified</th>
<th>Owner</th>
<th>Protections</th>
</tr>
</thead>
<tbody>
<tr>
<td>xyz.p</td>
<td>1</td>
<td>10</td>
<td>5</td>
<td>11/14/93</td>
<td>11/14/93</td>
<td>16</td>
<td>RWX by Owner</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>12</td>
<td>7</td>
<td>10:30:57</td>
<td>19:30:57</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>23</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ab.c</td>
<td>1</td>
<td>10</td>
<td>8</td>
<td>11/14/93</td>
<td>11/14/93</td>
<td>20</td>
<td>RX - All W-Owner</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>20</td>
<td>10</td>
<td>10:30:57</td>
<td>19:30:57</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>23</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>34</td>
<td>2</td>
<td>11/14/93</td>
<td>11/14/93</td>
<td>20</td>
<td>RX - All W-Owner</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>23</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>10</td>
<td>8</td>
<td>11/14/93</td>
<td>11/14/93</td>
<td>20</td>
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<td></td>
<td>1</td>
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<td>10</td>
<td>10:30:57</td>
<td>19:30:57</td>
<td></td>
<td></td>
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<td></td>
<td>2</td>
<td>23</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Creation Date: 11/14/93
Last Modified: 11/14/93
Owner: 16
Protections: RWX by Owner

R = Read
W = Write
X = Execute
Magnetic Tape

- A portion of a magnetic tape (adapted from [Hamacher, 1990]).
Magnetic Drum

- Fixed read/write heads (1 per track)
- Sector
- Tracks
Spiral Format for Compact Disk
ECMA-23 Keyboard Layout

- Keyboard layout for the ECMA-23 Standard (2nd ed.). Shift keys are frequently placed in the B row.
The Dvorak Keyboard Layout
Bit Pad with Puck

- Cable to host computer
- Puck
- Coil
- Buttons
Mouse and Trackball

- A three-button mouse (left) and a three-button trackball (right).
A user selects an object with a lightpen.
Touchscreen

- A user selects an object on a touchscreen.
Joystick

• A joystick with a selection button and a rotatable rod:
Laser Printer

- Schematic of a laser printer (adapted from [Tanenbaum, 1999]).

Page description from host computer → Page composing circuitry

Charged pattern → Stationary laser source

Toner cartridge → Rotating mirror

Cleaner and discharger

Heated rollers

Paper input ➔

Paper output ➔
Cathode Ray Tube

- A CRT with a single electron gun:
Display Controller

- Display controller for a 640×480 color monitor (adapted from [Hamacher et al., 1990]).